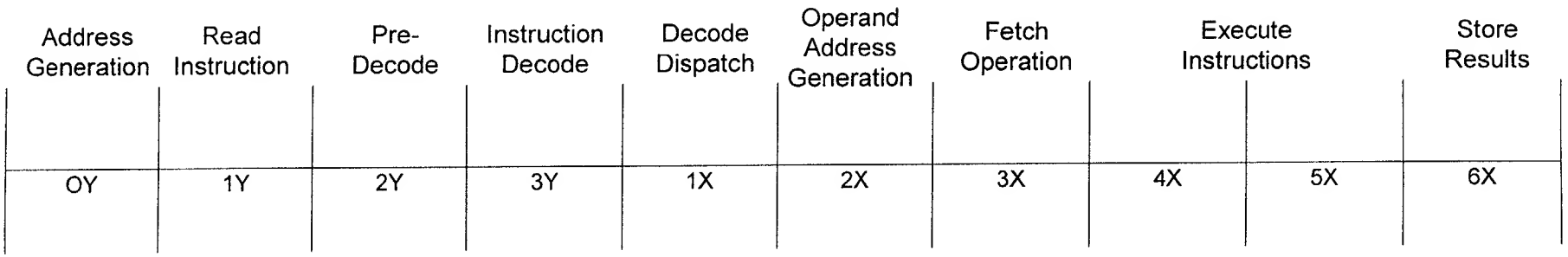
Address Generation
Read Instruction
Pre-Decode
Instruction Decode
Decode Dispatch
Operand Address Generation
Fetch Operation
Execute Instructions
Store Results
OY
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X

*FIG. 1*

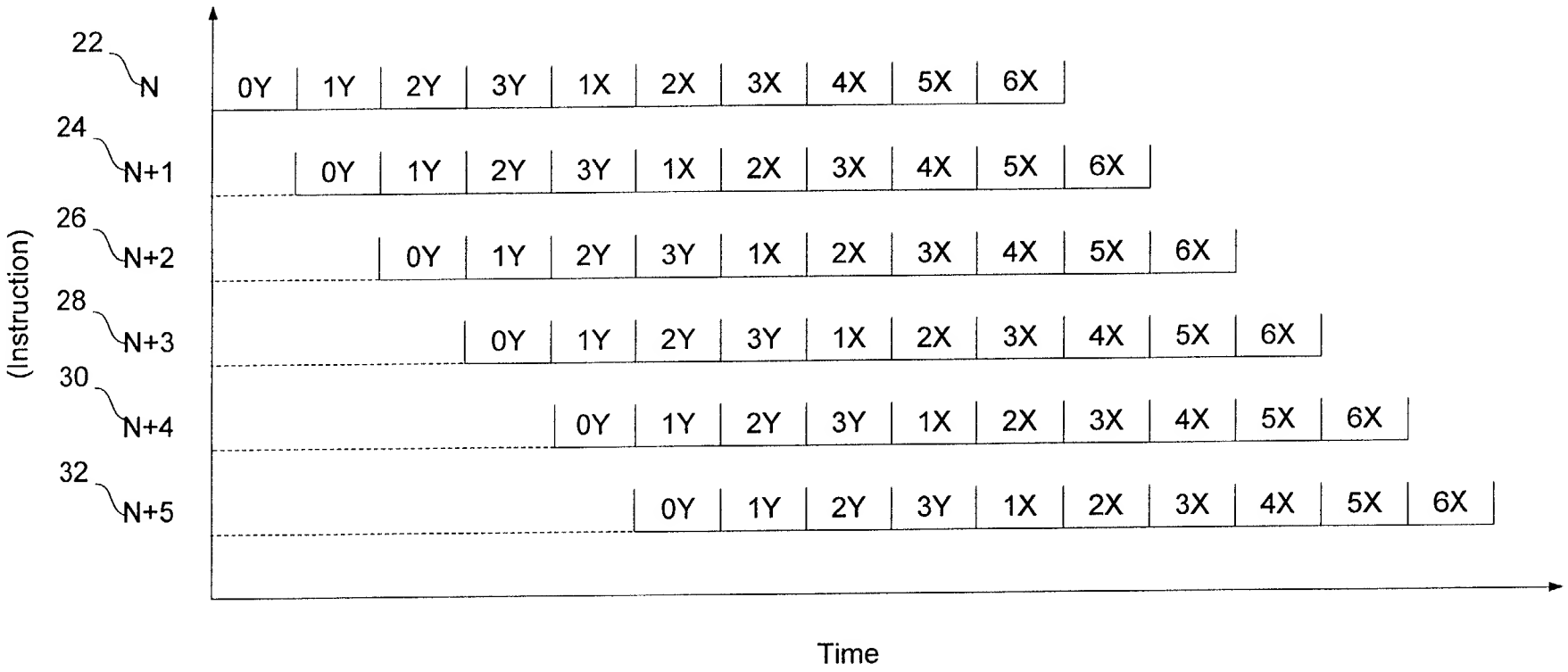
22
N
24
N+1
26
N+2
28
N+3
30
N+4
32
N+5
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
(Instruction)
Time

FIG. 2

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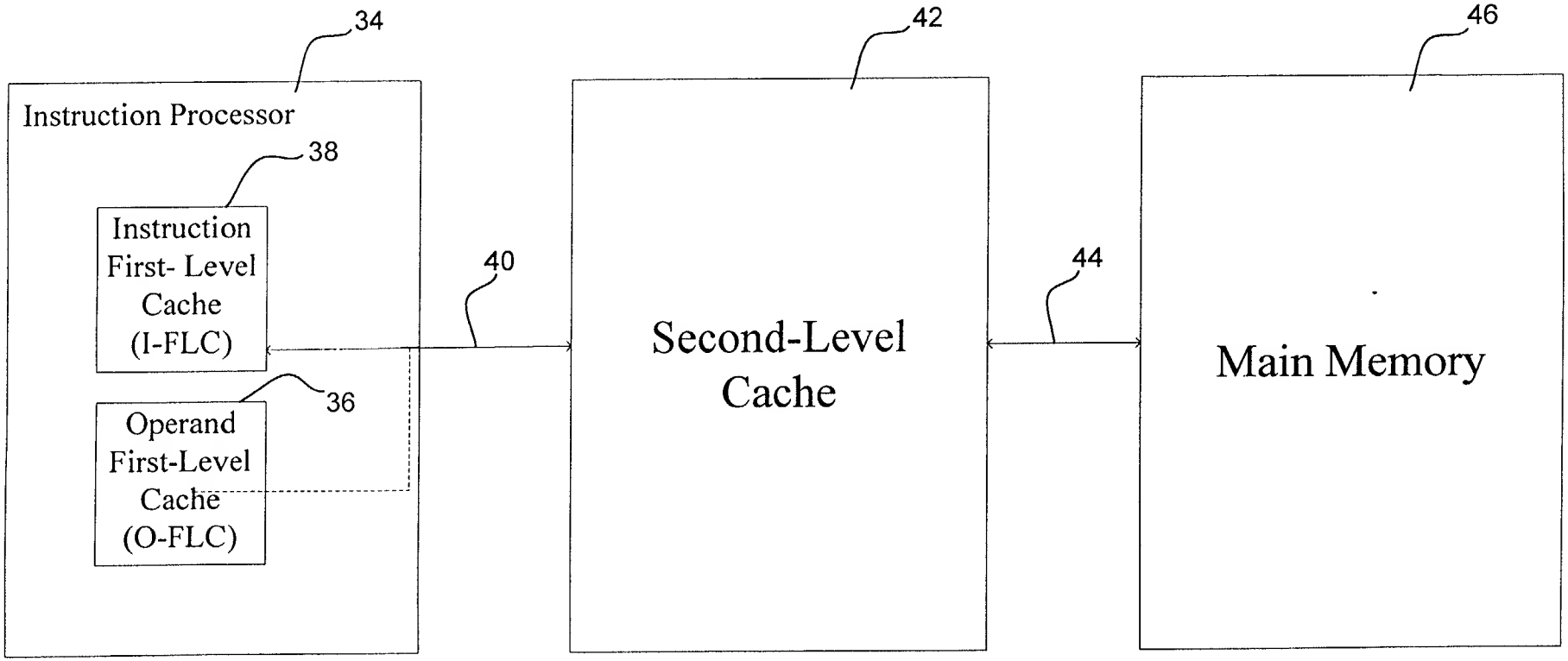



*FIG. 3*

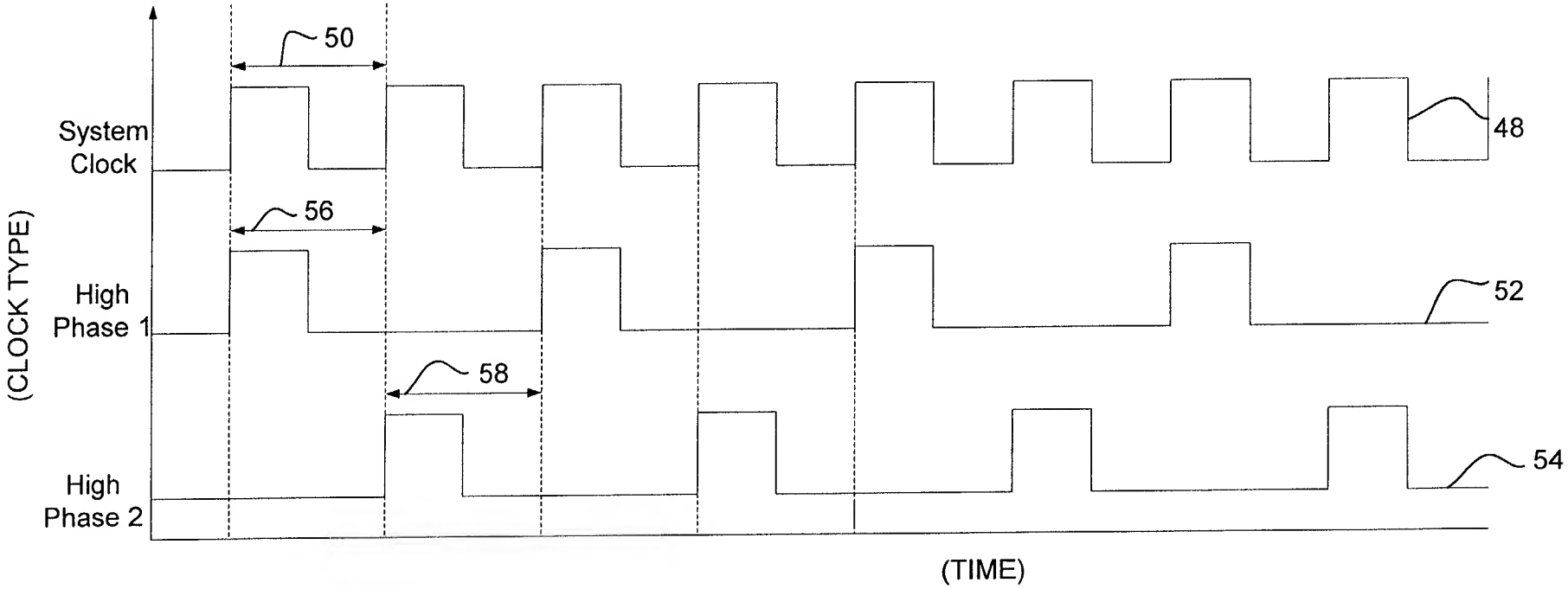

50
System Clock
48
56
High Phase 1
52
58
High Phase 2
54
(CLOCK TYPE)
(TIME)

*FIG. 4*

Datasheet

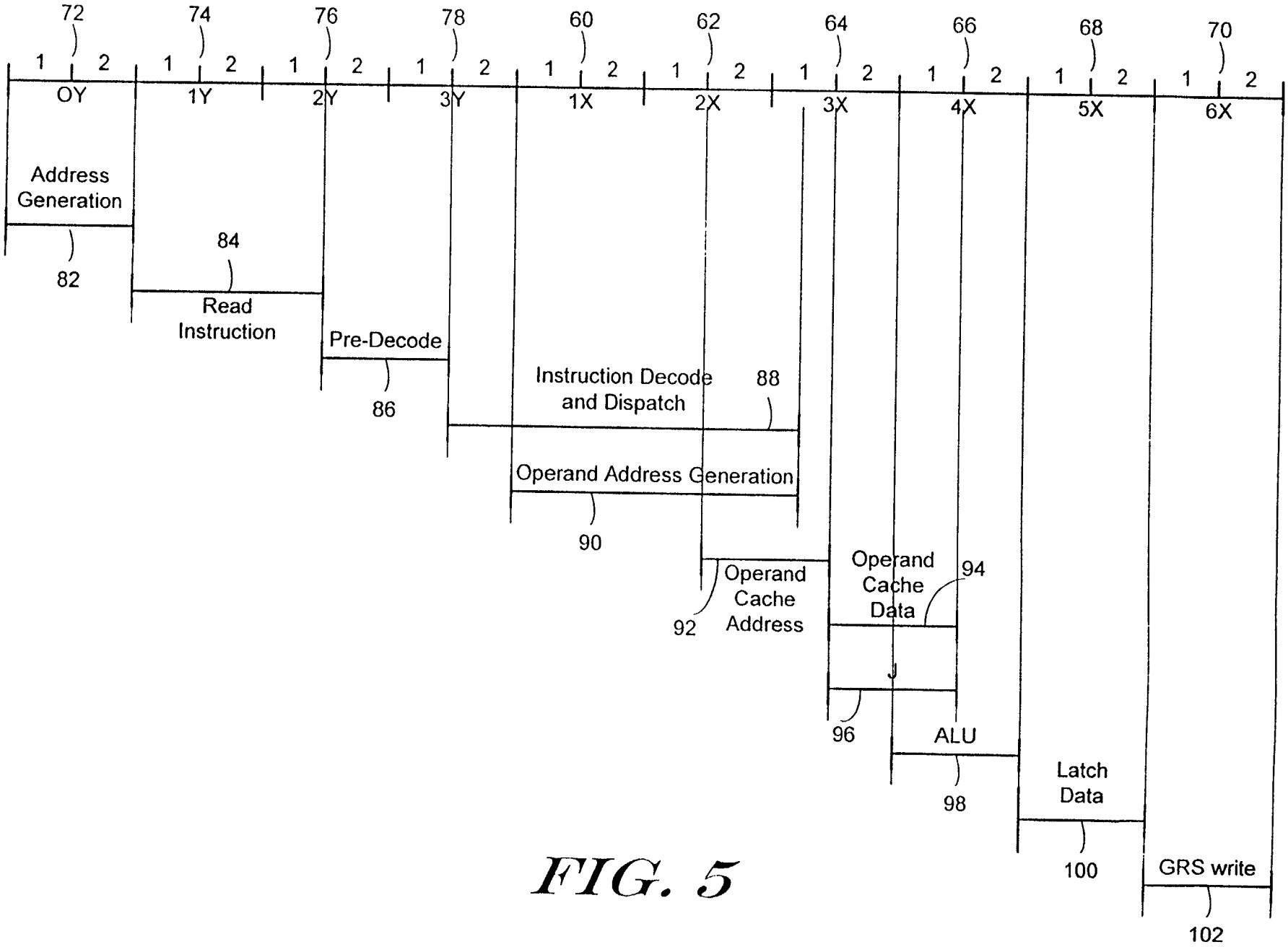



FIG. 5

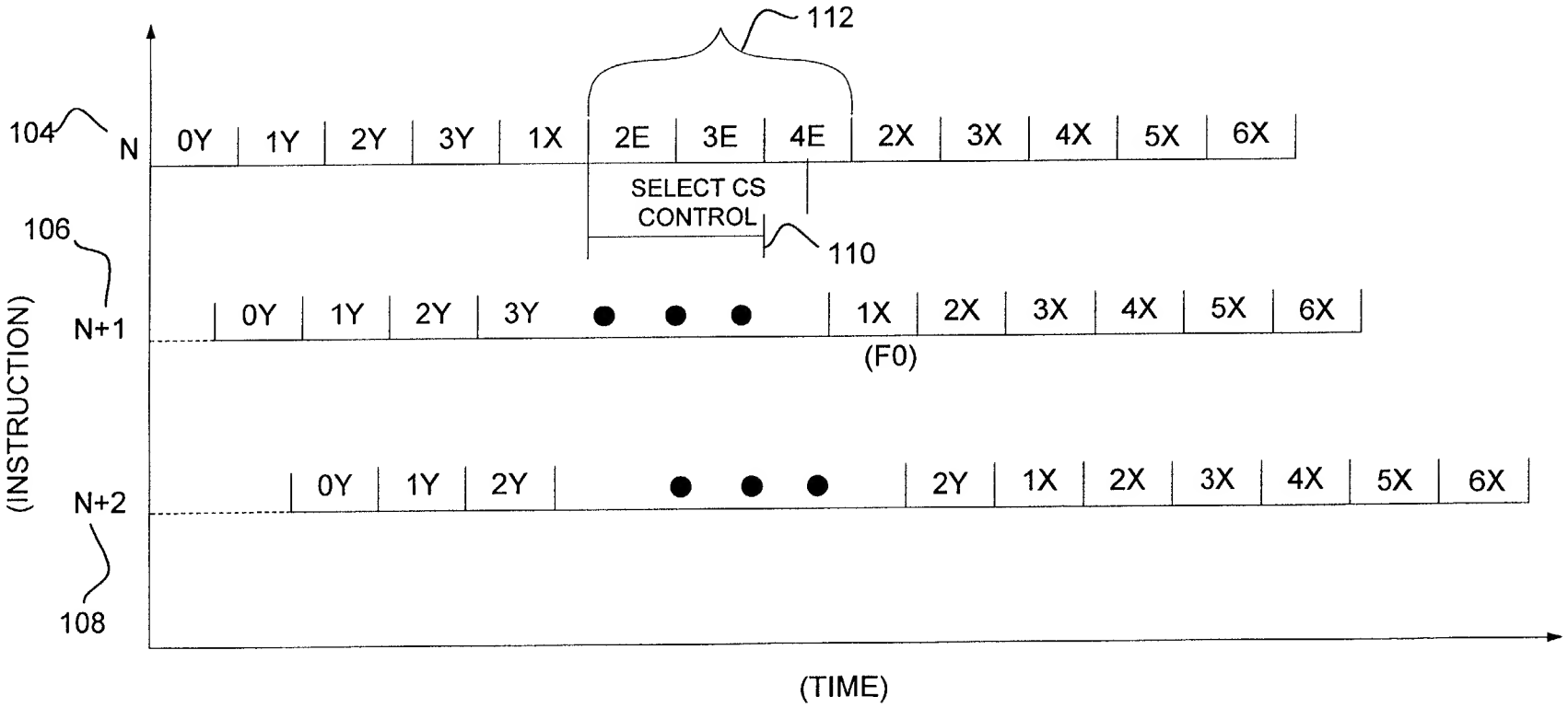
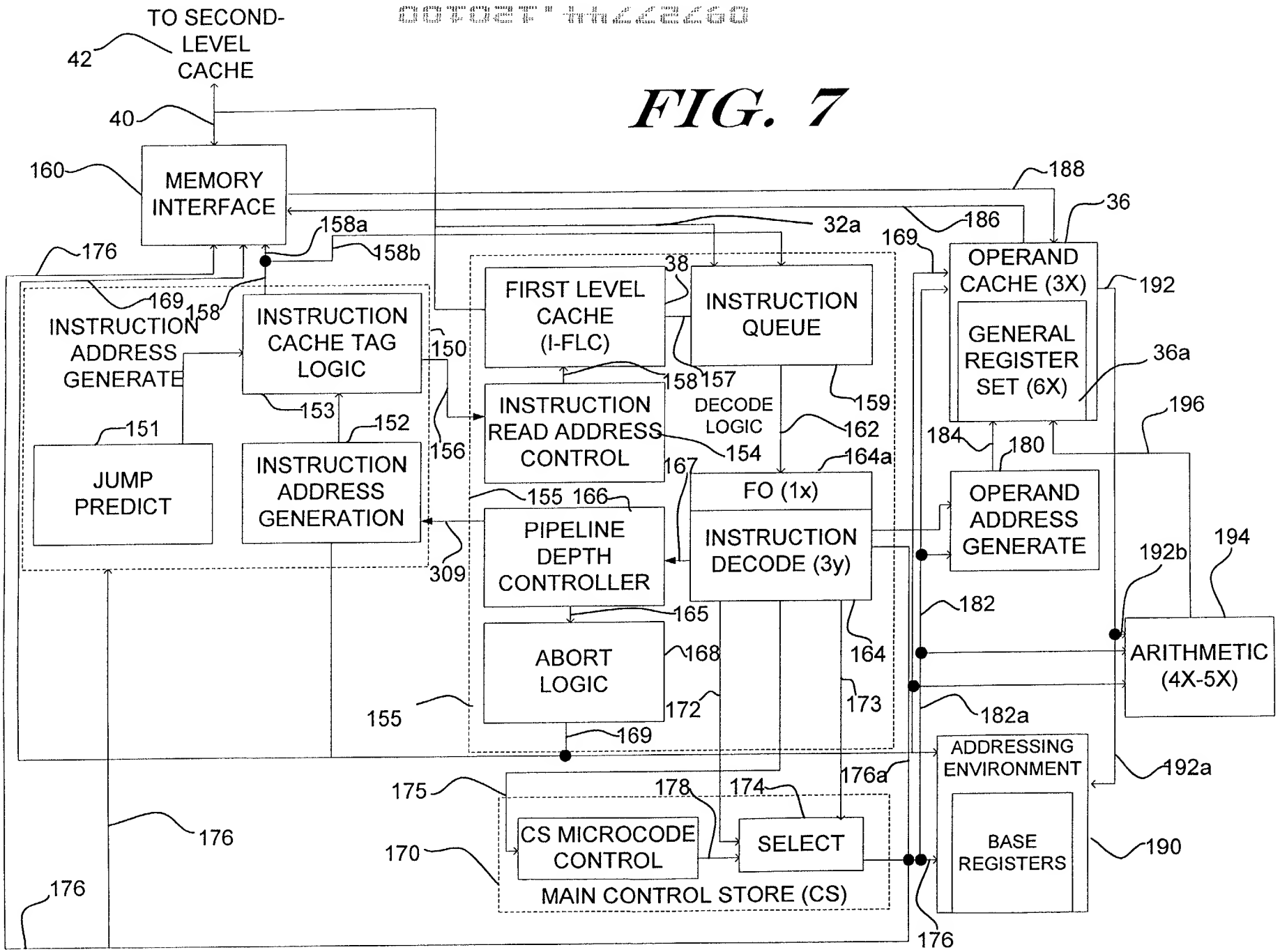

112
104
N
0Y
1Y
2Y
3Y
1X
2E
3E
4E
2X
3X
4X
5X
6X
SELECT CS CONTROL
110
106
N+1
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
(F0)
(INSTRUCTION)
N+2
0Y
1Y
2Y
2Y
1X
2X
3X
4X
5X
6X
108
(TIME)

FIG. 6

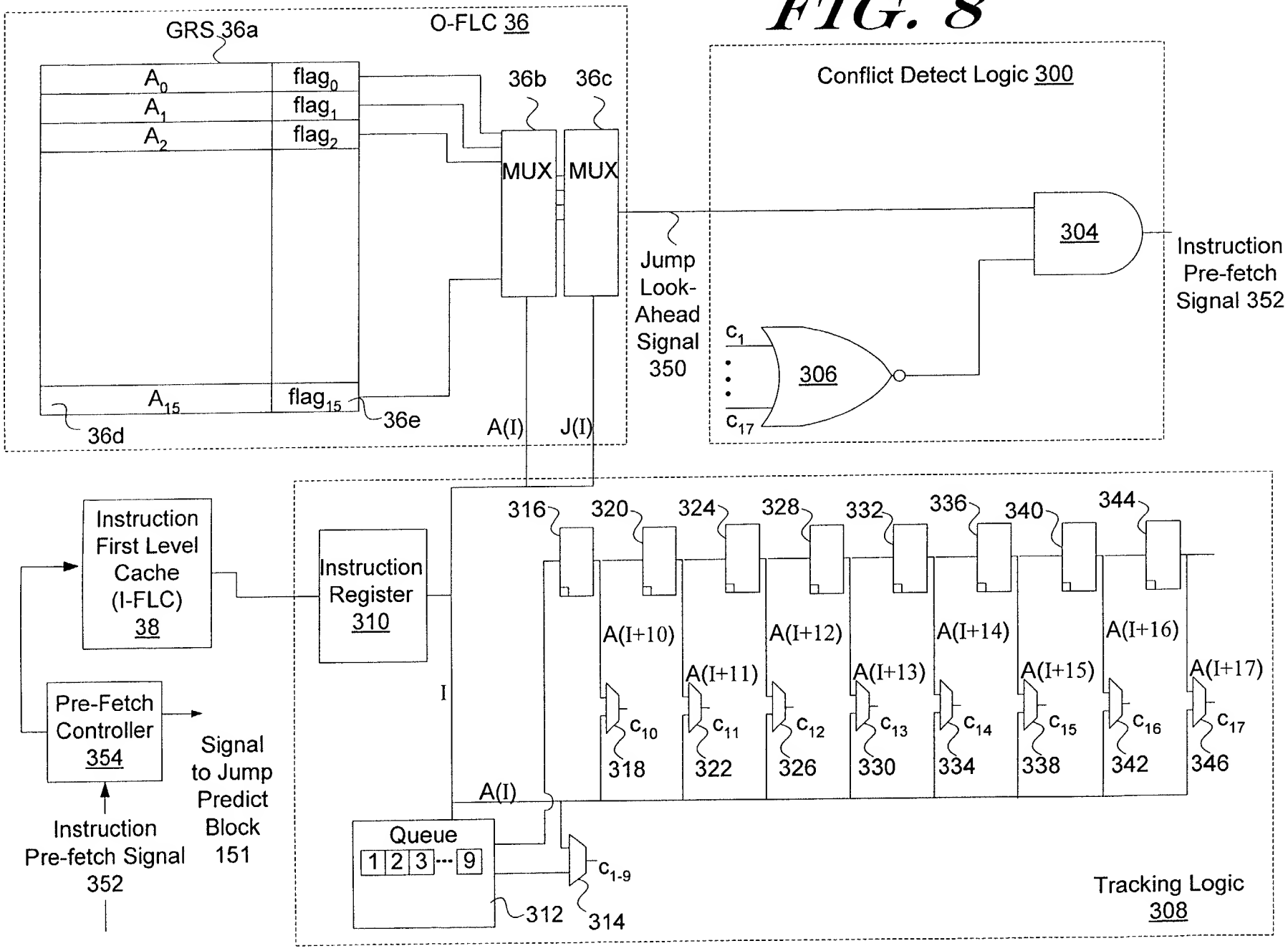
Patent Application Publication

# FIG. 7



patent application

FIG. 8



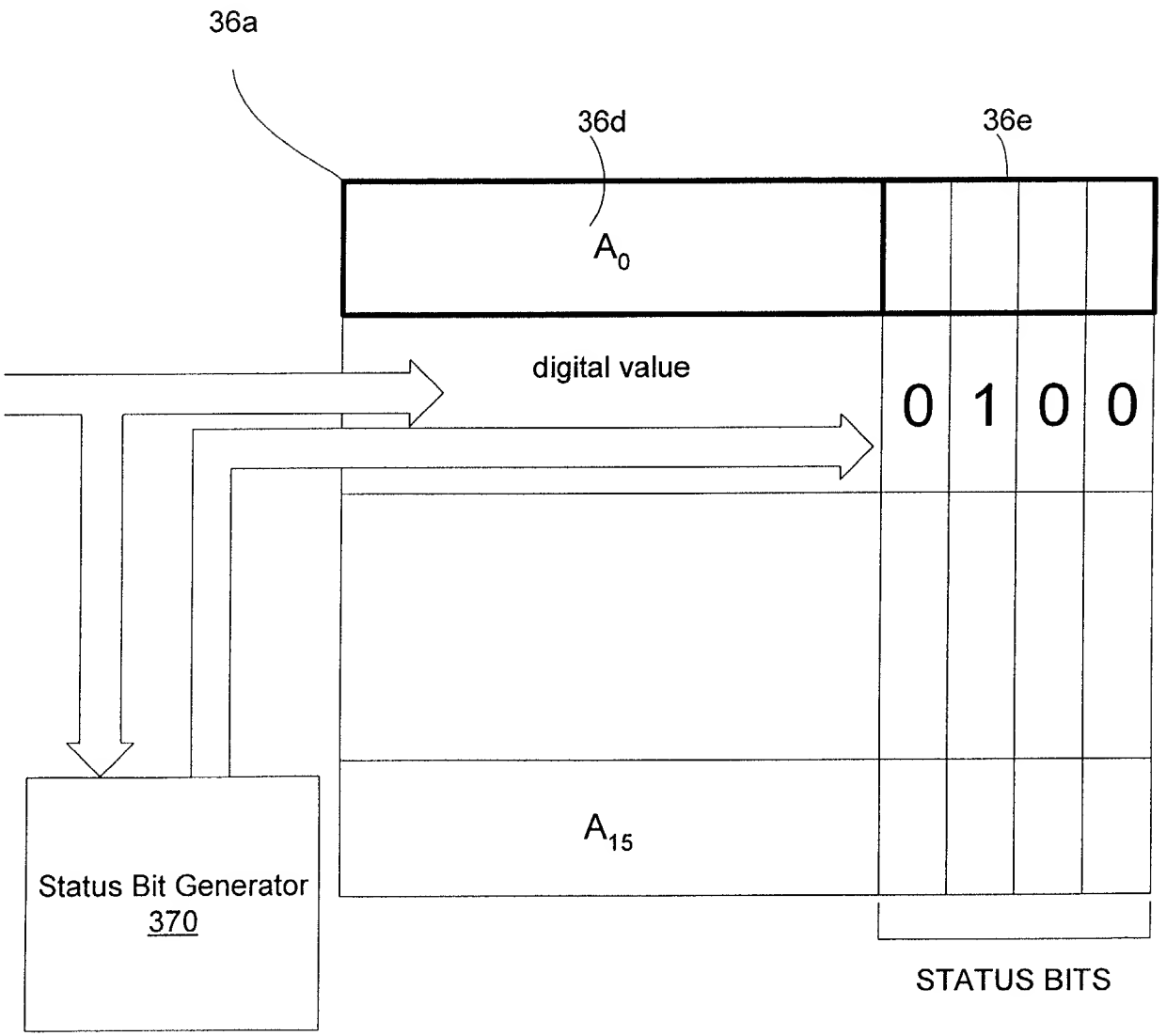

36a
36d
36e
$A_0$
digital value
0 1 0 0
$A_{15}$
Status Bit Generator
370
STATUS BITS

*FIG. 9*